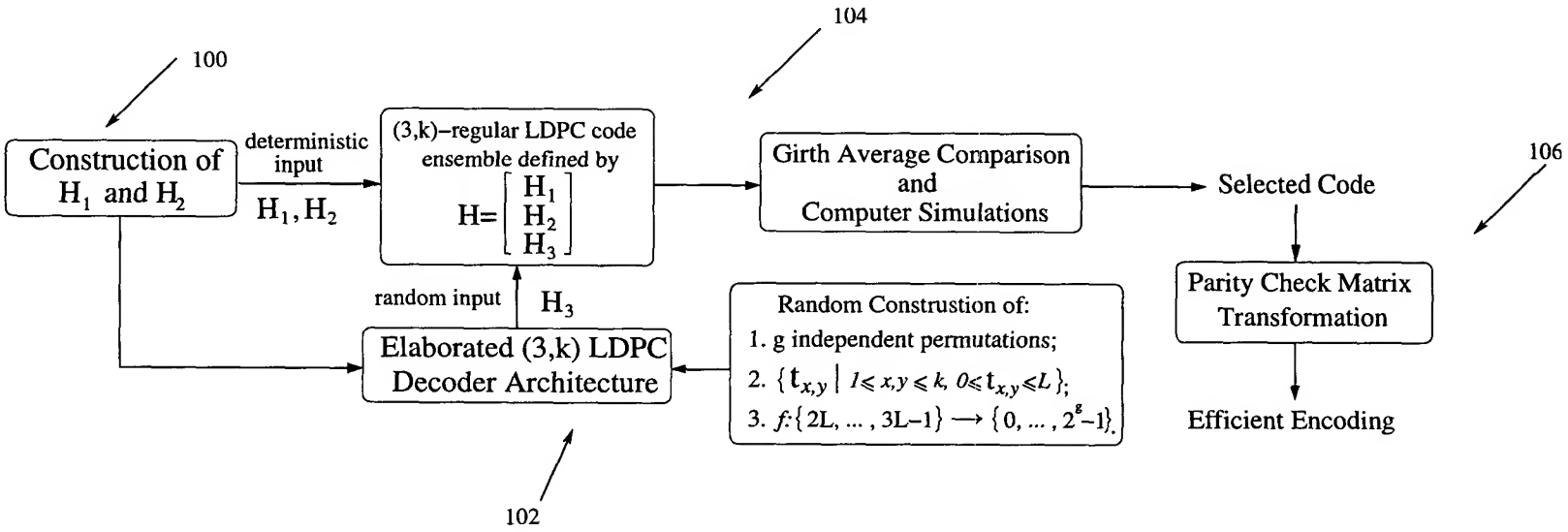
100
104
106
Construction of
H_1 and H_2
deterministic
input
H_1, H_2
(3,k)–regular LDPC code
ensemble defined by
$H=\begin{bmatrix} H_1 \\ H_2 \\ H_3 \end{bmatrix}$
Girth Average Comparison
and
Computer Simulations
Selected Code
Parity Check Matrix
Transformation
Efficient Encoding
random input
H_3
Elaborated (3,k) LDPC
Decoder Architecture
Random Construstion of:
1. g independent permutations;
2. $\{t_{x,y} \mid 1 \leq x,y \leq k,\ 0 \leq t_{x,y} \leq L\}$;
3. $f:\{2L, \ldots, 3L-1\} \longrightarrow \{0, \ldots, 2^g-1\}$.
102

Fig. 1

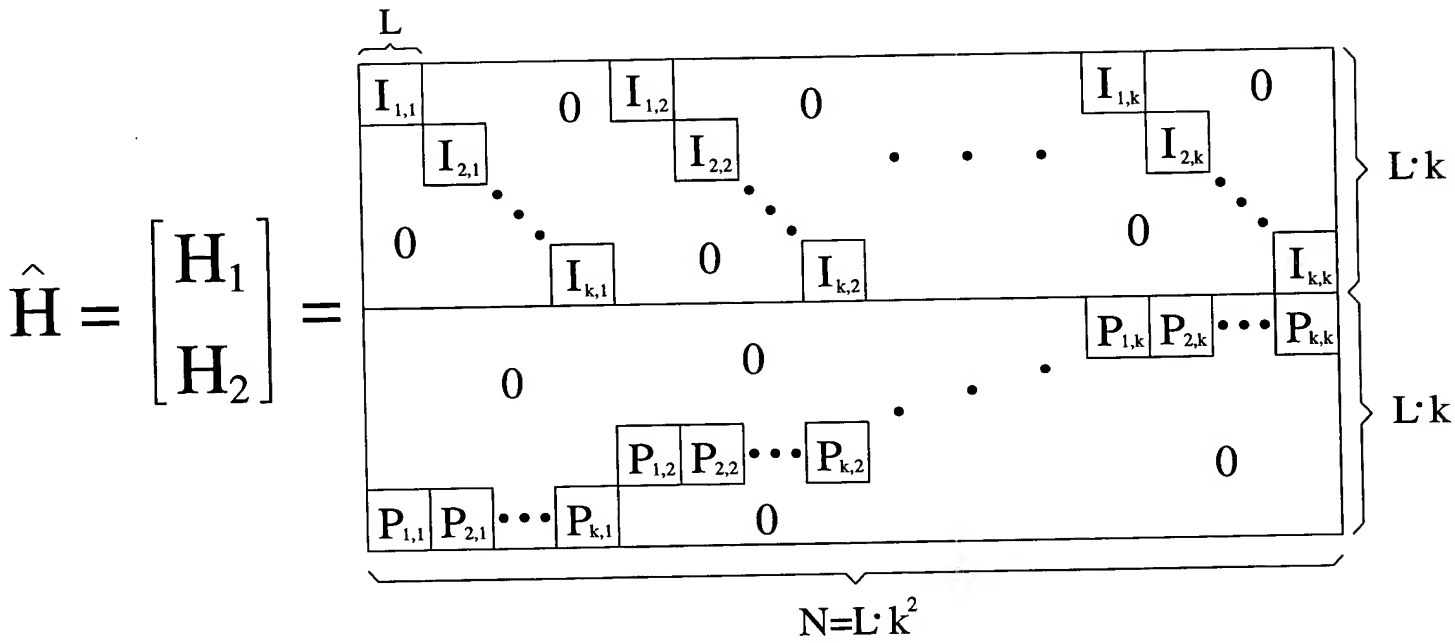
$\hat{H} = \begin{bmatrix} H_1 \\ H_2 \end{bmatrix}$
L
$I_{1,1}$ 0 $I_{1,2}$ 0 $I_{1,k}$ 0
$I_{2,1}$ $I_{2,2}$ $I_{2,k}$
0 0 0
$I_{k,1}$ $I_{k,2}$ $I_{k,k}$
$P_{1,k}$ $P_{2,k}$ $P_{k,k}$
0 0
$P_{1,2}$ $P_{2,2}$ $P_{k,2}$ 0
$P_{1,1}$ $P_{2,1}$ $P_{k,1}$ 0
L·k
L·k
$N=L\cdot k^2$

Fig. 2

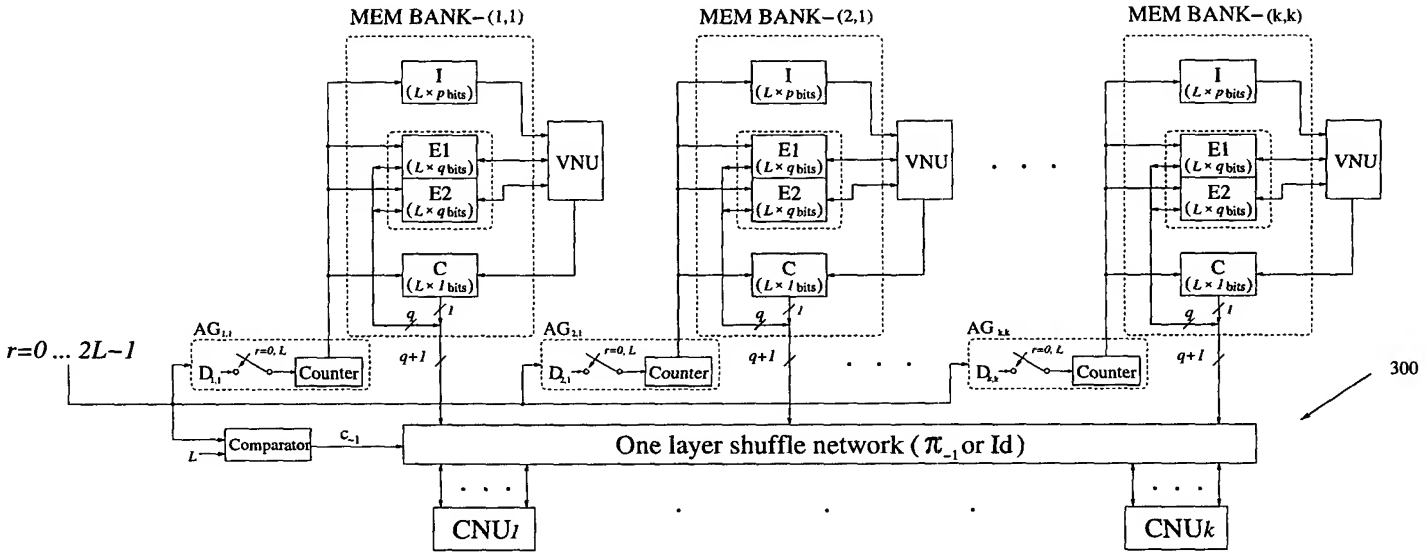
MEM BANK-(1,1)
MEM BANK-(2,1)
MEM BANK-(k,k)
I
(L × p bits)
E1
(L × q bits)
E2
(L × q bits)
C
(L × 1 bits)
VNU
q
1
q+1
r=0 ... 2L-1
AG1,1
AG2,1
AGk,k
r=0, L
Counter
Comparator
L
c-1
One layer shuffle network (π-1 or Id)
300
CNU1
CNUk

Fig. 3

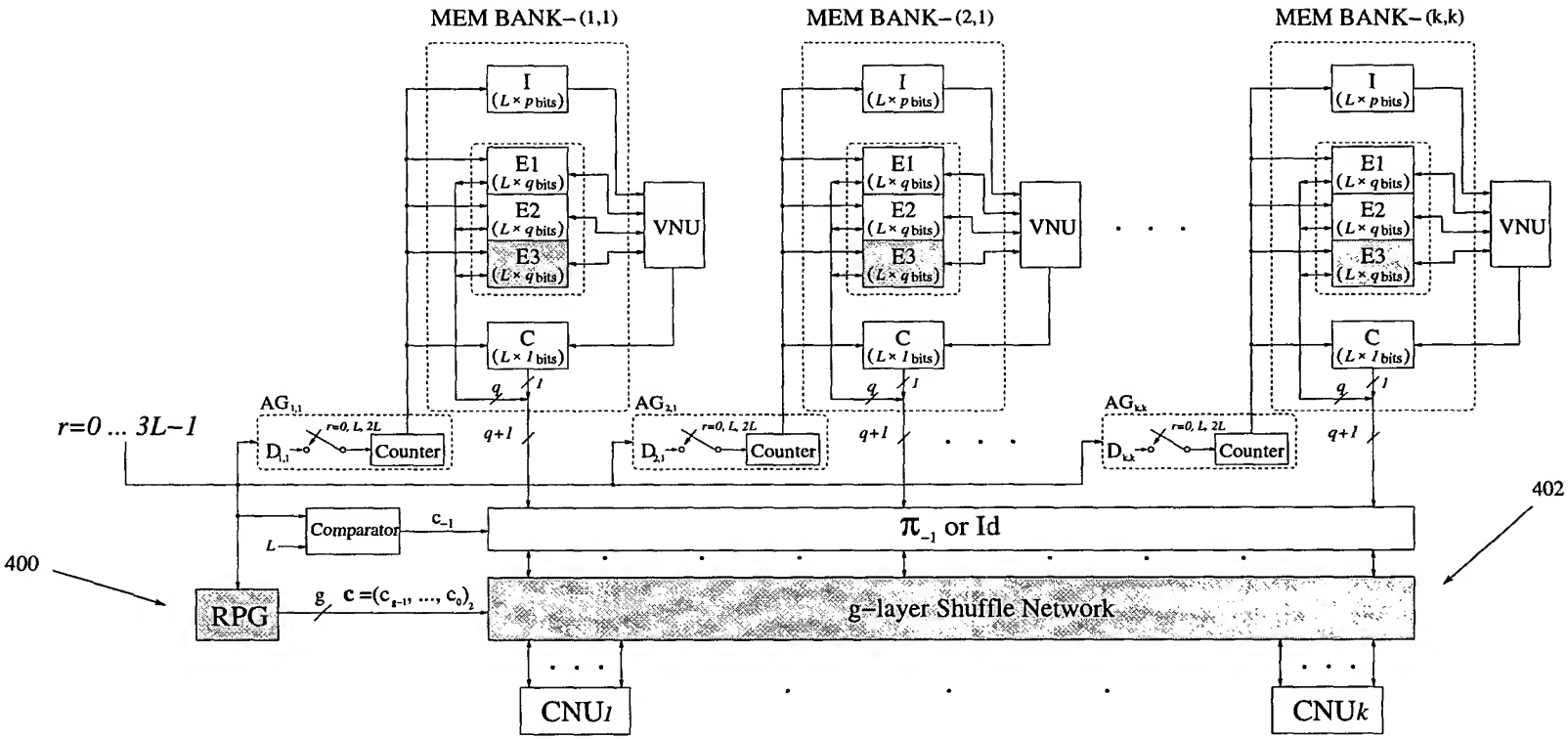
MEM BANK–(1,1)
MEM BANK–(2,1)
MEM BANK–(k,k)
I
(L × p bits)
E1
(L × q bits)
E2
(L × q bits)
E3
(L × q bits)
C
(L × 1 bits)
VNU
q
1
q+1
r=0 ... 3L–1
AG1,1
AG2,1
AGk,k
r=0, L, 2L
D1,1
D2,1
Dk,k
Counter
Comparator
L
c–1
π–1 or Id
400
402
RPG
g
c =(cg–1, ..., c0)2
g–layer Shuffle Network
CNU1
CNUk

Fig. 4

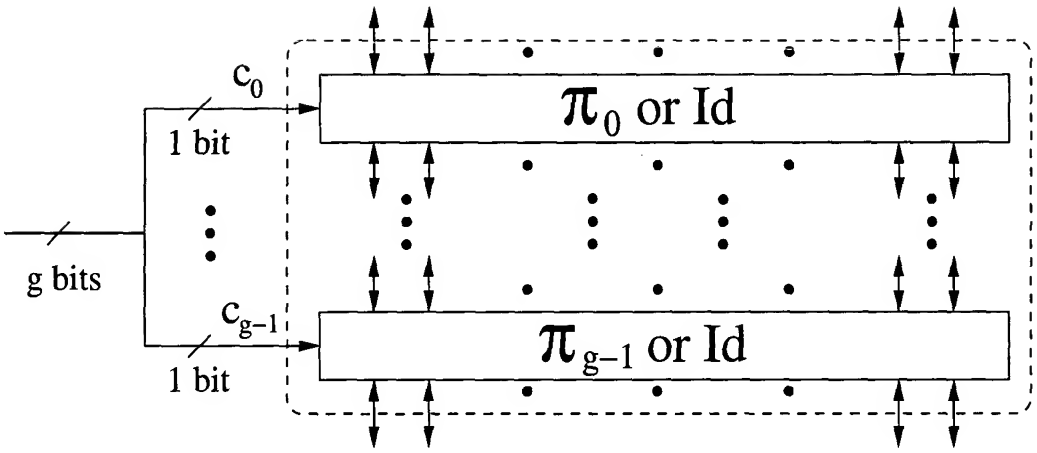

Fig. 5

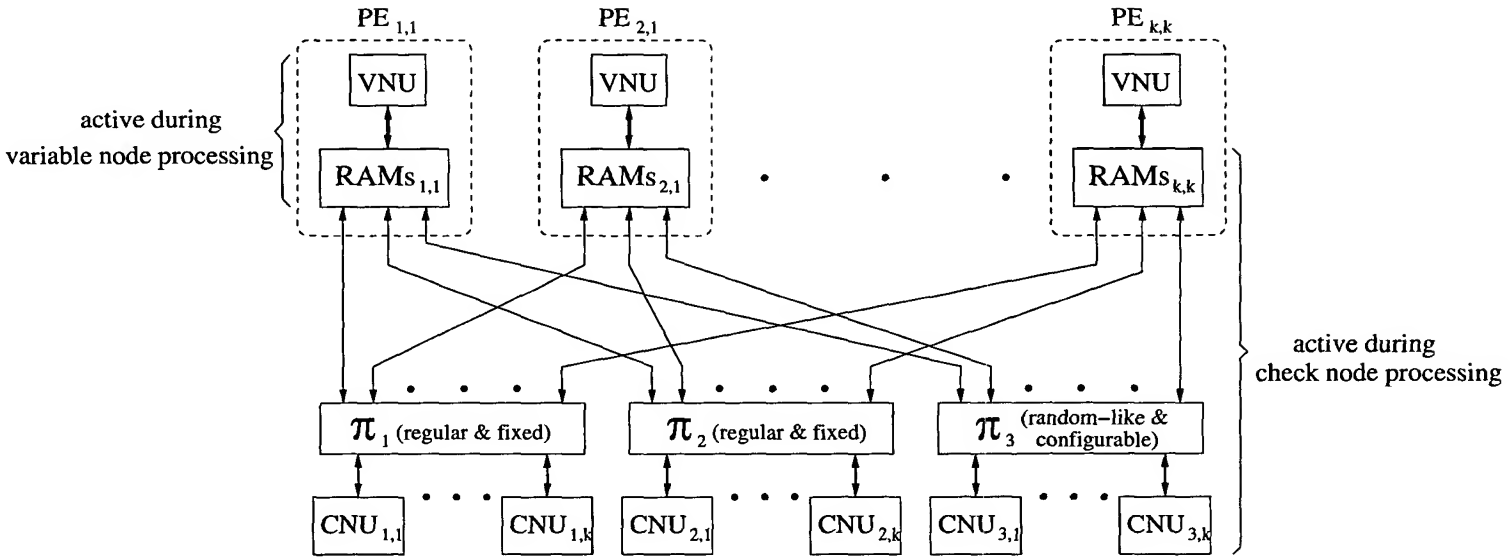
PE 1,1
PE 2,1
PE k,k
VNU
VNU
VNU
active during
variable node processing
RAMs 1,1
RAMs 2,1
RAMs k,k
active during
check node processing
π 1 (regular & fixed)
π 2 (regular & fixed)
π 3 (random–like & configurable)
CNU 1,1
CNU 1,k
CNU 2,1
CNU 2,k
CNU 3,1
CNU 3,k

Fig. 6

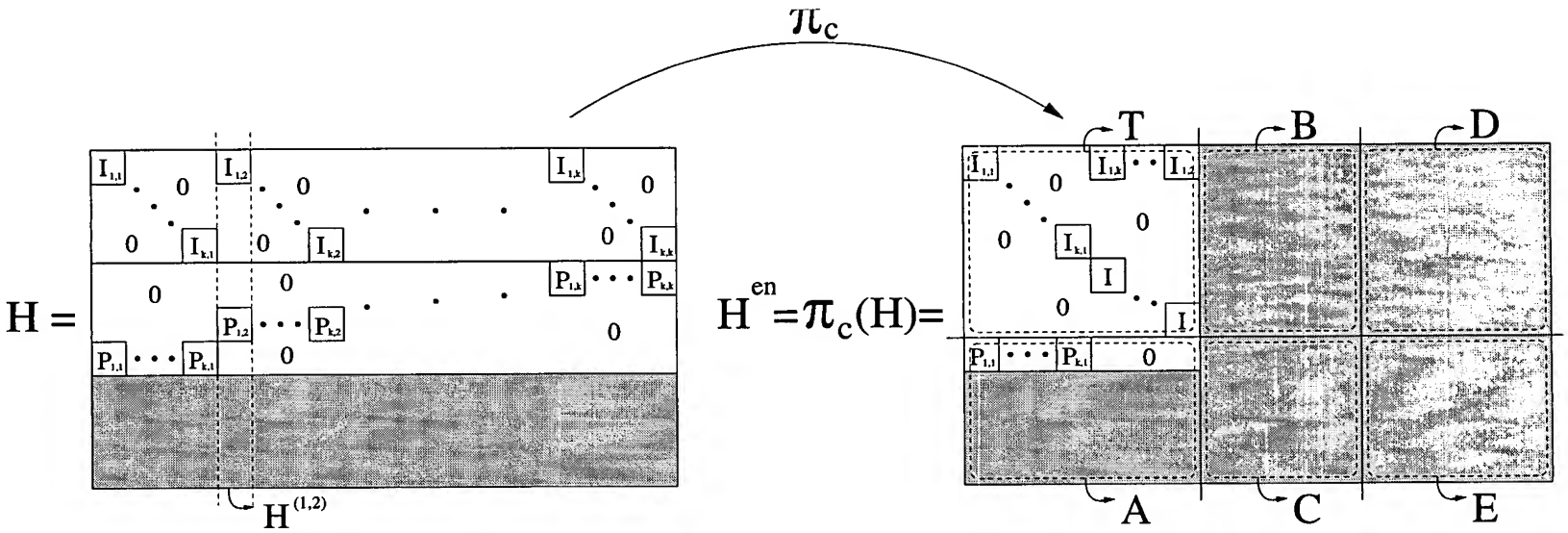

Fig. 7